LANSDALE Semiconductor, Inc.

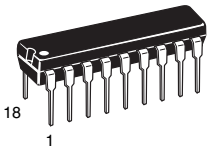
ML145106
PLL Frequency Synthesizer CMOS

INTERFACES WITH DUAL–MODULUS PRESCALERS

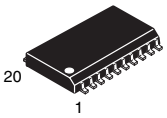
Legacy Device: *Motorola MC145106*

The ML145106 is a phase–locked loop (PLL) frequency synthesizer constructed in CMOS on a single monolithic structure. This synthesizer finds applications in such areas as AM radio, shortwave, amateur radio, CB and FM transceivers. The device contains an oscillator/amplifier, a 210 or 211 divider chain for the oscillator signal, a programmable divider chain for the input signal, and a phase detector. The ML145106 has circuitry for a 10.24 MHz oscillator or may operate with an external signal. The circuit provides a 5.12 MHz output signal, which can be used for frequency tripling. A 2^9 programmable divider divides the input signal frequency for channel selection. The inputs to the programmable divider are standard ground–to–supply binary signals. Pull–down resistors on these inputs normally set these inputs to ground enabling these programmable inputs to be controlled from a mechanical switch or electronic circuitry.

The phase detector may control a VCO and yields a high level signal when input frequency is low, and a low level signal when input frequency is high. An out–of–lock signal is provided from the on–chip lock detector with a "0" level for the out–of–lock condition.



P DIP 18 = VP
PLASTIC DIP
CASE 707



SOG 20W = -6P
SOG PACKAGE
CASE 751D

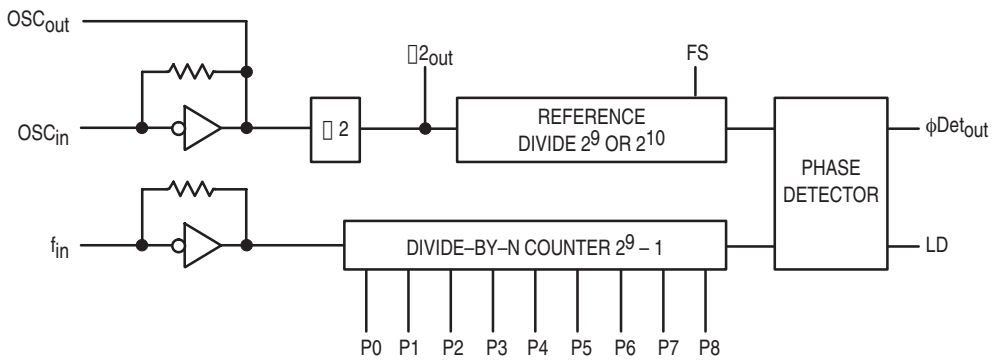
CROSS REFERENCE/ORDERING INFORMATION

PACKAGE	MOTOROLA	LANSDALE
P DIP 18	MC145106P	ML145106VP
SOG 20W	MC145106DW	ML145106-6P

Note: Lansdale lead free (**Pb**) product, as it becomes available, will be identified by a part number prefix change from **ML** to **MLE**.

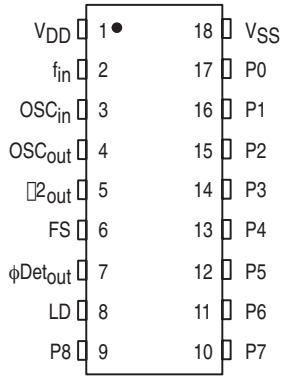
- Single Power Supply
- Wide Supply Range: 4.5 to 12 V
- Provision for 10.24 MHz Crystal Oscillator
- 5.12 MHz Output
- Programmable Division Binary Input Selects up to 2^9
- On–Chip Pull–Down Resistors on Programmable Divider Inputs
- Selectable Reference Divider, 2^{10} or 2^{11} (Including ÷ 2)
- Three–State Phase Detector
- See Application Note AN535 and Article Reprint AR254
- Chip Complexity: 880 FETs or 220 Equivalent Gates

BLOCK DIAGRAM

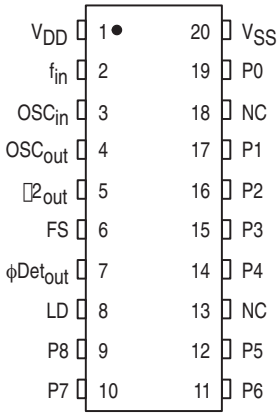


PIN ASSIGNMENTS

PLASTIC DIP



SOG PACKAGE



NC = NO CONNECTION

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Parameter	Symbol	Value	Unit
DC Supply Voltage	V_{DD}	– 0.5 to + 12	V
Input Voltage, All Inputs	V_{in}	– 0.5 to V_{DD} + 0.5	V
DC Input Current, per Pin	I	± 10	mA
Operating Temperature Range	T_A	– 40 to + 85	□C
Storage Temperature Range	T_{stg}	– 65 to + 150	□C

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum rated voltages to this high impedance circuit. For proper operation it is recommended that V_{in} and V_{out} be constrained to the range V_{SS}□≤(V_{in} or V_{out})□≤V_{DD}.

ELECTRICAL CHARACTERISTICS (T_A = 25°C Unless Otherwise Stated, Voltages Referenced to V_{SS})

Characteristic	Symbol	V_{DD} Vdc	All Types			Unit
			Min	Typ*	Max	
Power Supply Voltage Range	V_{DD}	–	4.5	–	12	V
Supply Current	I_{DD}	5.0	–	6	10	mA
		10	–	20	35	
		12	–	28	50	
Input Voltage "0" Level	V_{IL}	5.0	–	–	1.5	V
		10	–	–	3.0	
		12	–	–	3.6	
"1" Level	V_{IH}	5.0	3.5	–	–	
		10	7.0	–	–	
		12	8.4	–	–	
Input Current "0" Level FS, Pull–Up Resistor Source Current)	I_{in}	5.0	– 5.0	– 20	– 50	μA
		10	– 15	– 60	– 150	
		12	– 20	– 80	– 200	
(P0 – P8)		5.0	–	–	– 0.3	
		10	–	–	– 0.3	
		12	–	–	– 0.3	
(FS) "1" Level		5.0	–	–	0.3	
		10	–	–	0.3	
		12	–	–	0.3	
(P0 – P8, Pull–Down Resistor Sink Current)		5.0	7.5	30	75	
		10	22.5	90	225	
		12	30	120	300	
(OSC_{in}, f_{in}) "0" Level		5.0	– 2.0	– 6.0	– 15	
		10	– 6.0	– 25	– 62	
		12	– 9.0	– 37	– 92	
(OSC_{in}, f_{in}) "1" Level		5.0	2.0	6.0	15	
		10	6.0	25	62	
		12	9.0	37	92	
Output Drive Current	I_{OH}					mA
(V_O = 4.5 V) Source		5.0	– 0.7	– 1.4	–	
(V_O = 9.5 V)		10	– 1.1	– 2.2	–	
(V_O = 11.5 V)		12	– 1.5	– 3.0	–	
(V_O = 0.5 V) Sink	I_{OL}	5.0	0.9	1.8	–	
(V_O = 0.5 V)		10	1.4	2.8	–	
(V_O = 0.5 V)		12	2.0	4.0	–	
Input Amplitude	–					V p–p
(f_{in} @ 4.0 MHz)		–	1.0	0.2	–	Sine
(OSC_{in} @ 10.24 MHz)		–	1.5	0.3	–	
Input Resistance	R_{in}					MΩ
(OSC_{in}, f_{in})		5.0	–	1.0	–	
		10	–	0.5	–	
		12	–	–	–	
Input Capacitance (OSC_{in}, f_{in})	C_{in}	–	–	6.0	–	pF
Three–State Leakage Current	I_{OZ}	5.0	–	–	1.0	μA
(ϕDet_{out})		10	–	–	1.0	
		12	–	–	1.0	
Input Frequency	f_{in}	4.5	0	–	4.0	MHz
(– 40 to + 85°C)		12	0	–	4.0	
Oscillator Frequency	OSC_{in}	4.5	0.1	–	10.24	MHz
(– 40 to + 85°C)		12	0.1	–	10.24	

*Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TYPICAL CHARACTERISTICS*

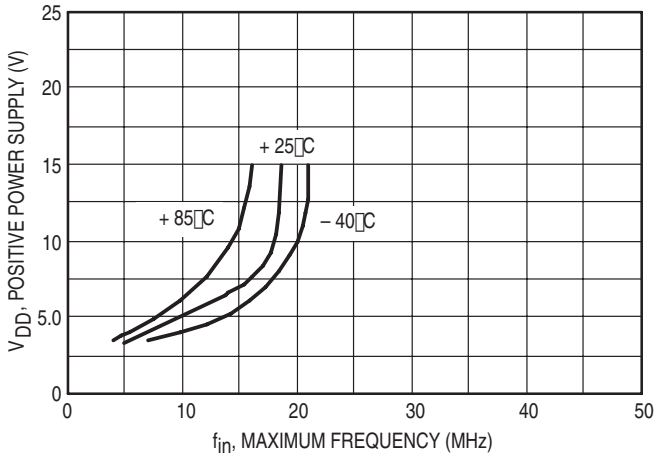


Figure 1. Maximum Divider Input Frequency versus Supply Voltage

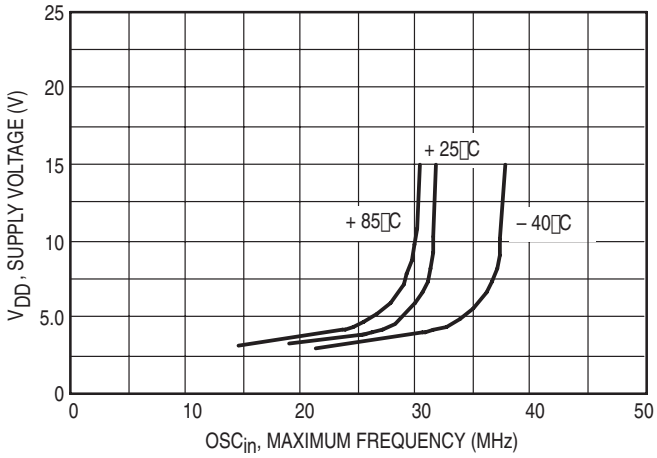


Figure 2. Maximum Oscillator Input Frequency versus Supply Voltage

* Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC's potential performance.

TRUTH TABLE

Selection									
P8	P7	P6	P5	P4	P3	P2	P1	P0	Divide by N
0	0	0	0	0	0	0	0	0	2*
0	0	0	0	0	0	0	0	1	3*
0	0	0	0	0	0	0	1	0	2
0	0	0	0	0	0	0	1	1	3
0	0	0	0	0	0	1	0	0	4
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
0	1	1	1	1	1	1	1	1	255
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
•	•	•	•	•	•	•	•	•	•
1	1	1	1	1	1	1	1	1	511

1: Voltage level = V_{DD}.
0: Voltage level = 0 or open circuit input.
* The binary setting of 00000000 and 00000001 on P8 to P0 results in a 2 and 3 division which is not in the 2^N – 1 sequence. When pin is not connected the logic signal on that pin can be treated as a “0”.

PIN DESCRIPTIONS

P0 – P8
Programmable Inputs (PDIP – Pins 17 – 9; SOG – Pins 19, 17 – 14, 12 – 9)
Programmable divider inputs (binary).

fin
Frequency Input (PDIP, SOG – Pin 2)
Frequency input to programmable divider (derived fromVCO).

OSC_{in}, OSC_{out}
Oscillator Input and Oscillator Output (PDIP, SOG – Pins 3, 4)
Oscillator/amplifier input and output terminals.

LD
Lock Detector (PDIP, SOG – Pin 8)
LD is high when loop is locked, pulses low when out–of–lock.

ϕDet_{out} (PDIP, SOG – Pin 7)
Signal for control of external VCO, output high when f_{in}/N is less than the reference frequency; output low when f_{in}/N is greater than the reference frequency. Reference frequency is the divided down oscillator–input frequency typically 5.0 or 10 kHz.

NOTE
Phase Detector Gain = VDD/4π.

FS
Reference Oscillator Frequency Division Select (PDIP,SOG – Pin 6)
When using 10.24 MHz OSC frequency, this control selects 10 kHz, a “0” selects 5.0 kHz.

$\div 2_{out}$ (PDIP, SOG – Pin 5)
Reference OSC frequency divided by 2 output; when using 10.24 MHz OSC frequency, this output is 5.12 MHz for frequency tripling applications.

V_{DD}
Positive Power Supply (PDIP, SOG – Pin 1)

V_{SS}
Ground (PDIP – Pin 18, SOG – Pin 20)

Legacy Applications Information

PLL SYNTHESIZER APPLICATIONS

The ML145106 is well suited for applications in CB radios because of the channelized frequency requirements. A typical 40 channel CB transceiver synthesizer, using a single crystal reference, is shown in Figure 3 for receiver IF values of 10.695 MHz and 455 kHz.

In addition to applications in CB radios, the MC145106 can be used as a synthesizer for several other systems. Various frequency spectrums can be achieved through the use of proper offset, prescaling, and loop programming techniques. In general, 300 – 400 channels can be synthesized using a single loop, with many additional channels available when multiple loop approaches are employed. Figures 4 and 5 are examples of some possibilities.

In the aircraft synthesizer of Figure 5, the VHF loop (top) will provide a 50 kHz, 360 channel system with 10.7 MHz R/T offset when only the 11.0500 MHz (transmit) and 12.1200 MHz (receive) frequencies are provided to mixer #1. When these signals are provided with crystal oscillators, the result is a three crystal 360 channel, 50 kHz step synthesizer. When using the offset loop (bottom) in Figure 5 to provide the indicated injection frequencies for mixer #1 (two for transmit and two for receive) 360 additional channels are possible. This results in a 720–channel, 25 kHz step synthesizer which requires only two crystals and provides R/T offset capability. The receive offset value is determined by the 11.31 MHz crystal frequency and is 10.7 MHz for the example.

The VHF marine synthesizer in Figure 4 depicts a single loop approach for FM transceivers. The VCO operates on frequency during transmit and is offset downward during receive. The offset corresponds to the receive IF (10.7 MHz) for channels having identical receive/transmit frequencies (simplex), and is (10.7 – 4.6 = 6.1) MHz for duplex channels. Carrier modulation is introduced in the loop during transmit.

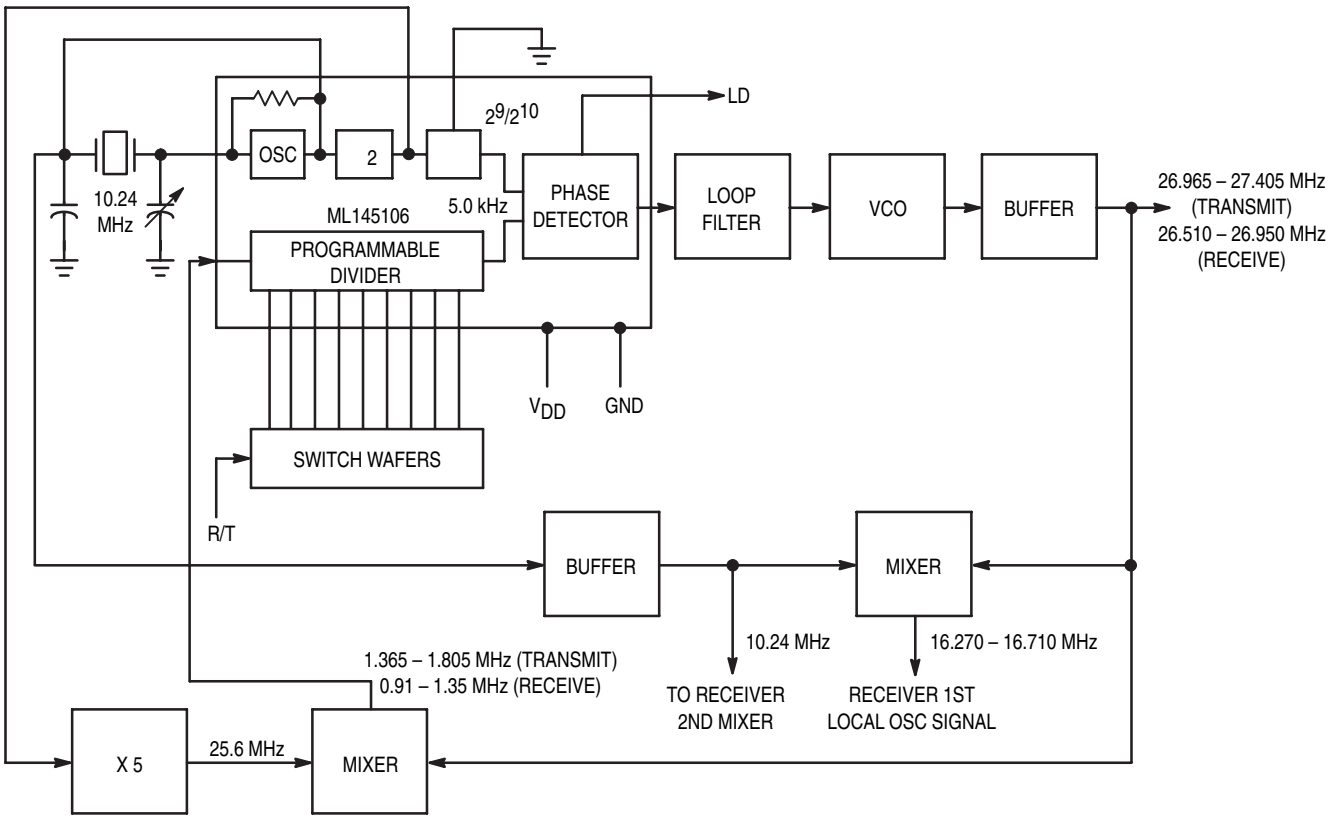
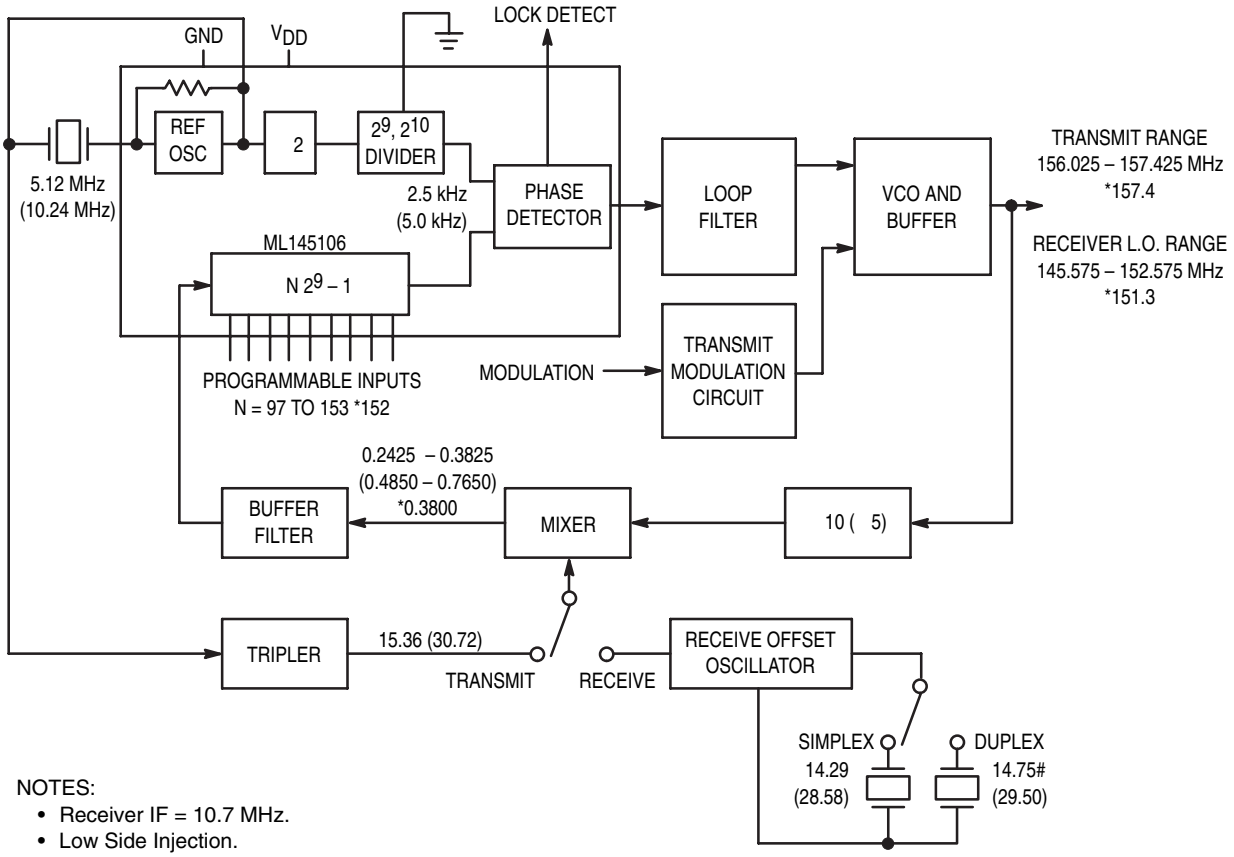


Figure 3. Single Crystal CB Synthesizer Featuring On–Frequency VCO During Transmit

Legacy Applications Information



NOTES:
- Receiver IF = 10.7 MHz.
- Low Side Injection.
- Duplex Offset = 4.6 MHz.
- Step Size = 25 kHz.
- Frequencies in MHz unless noted.
- Values in parentheses are for a 5.0 kHz reference frequency.
- Example frequencies for Channel 28 shown by *.

#Can be eliminated by adding 184 to N for Duplex Channels.

Figure 4. VHF Marine Transceiver Synthesizer

Legacy Applications Information

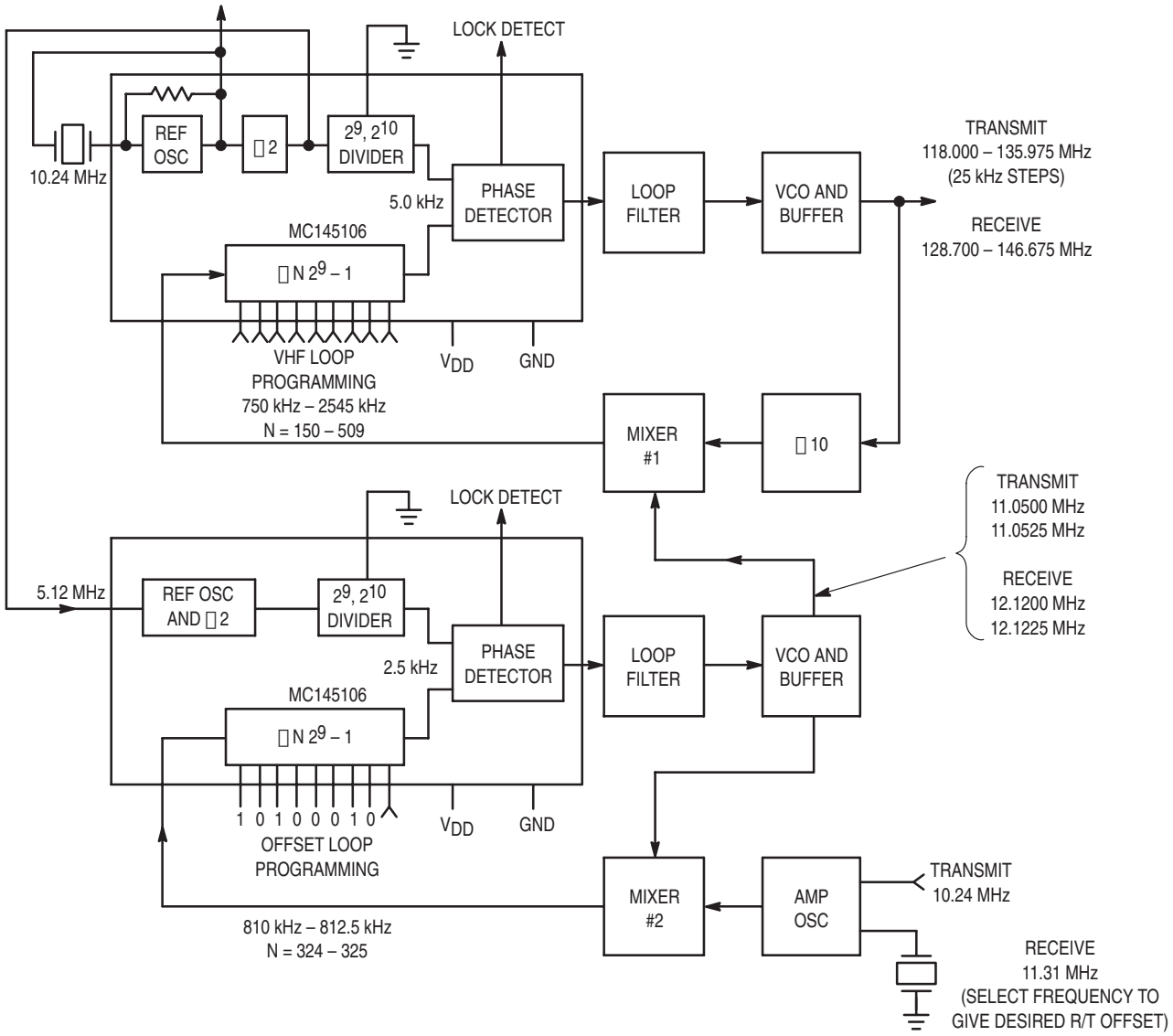
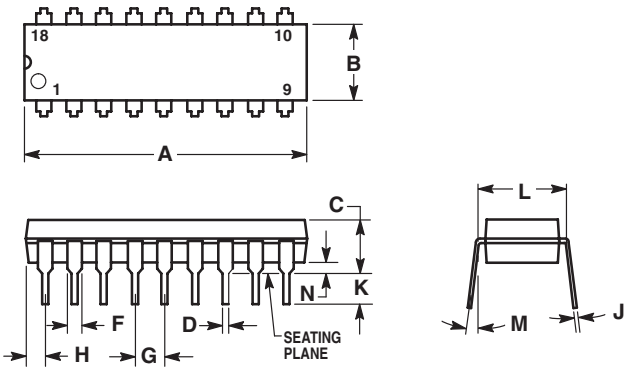


Figure 5. VHF Aircraft 720 Channel Two Crystal Frequency Synthesizer

OUTLINE DIMENSIONS

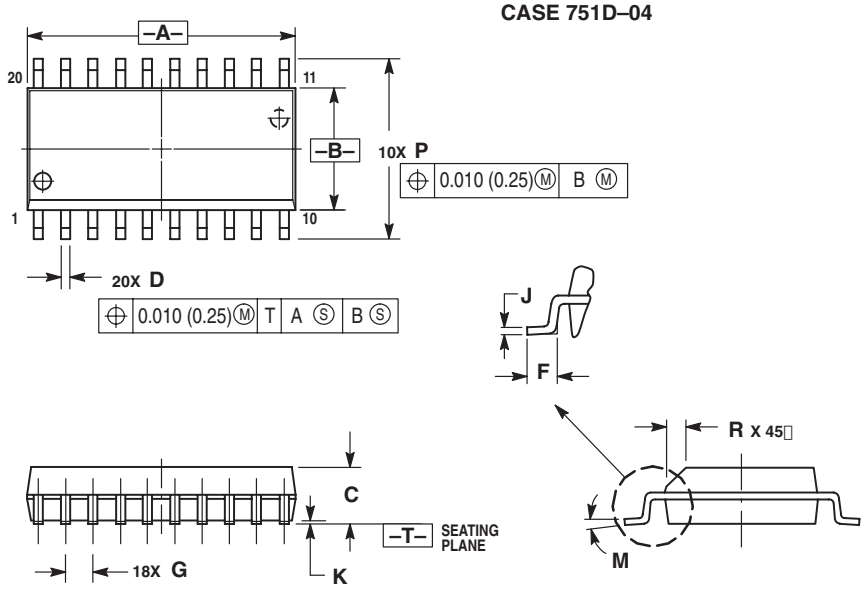
P DIP 18 = VP
(ML145106VP)
CASE 707–02



NOTES:
1. POSITIONAL TOLERANCE OF LEADS (D), SHALL BE WITHIN 0.25 (0.010) AT MAXIMUM MATERIAL CONDITION, IN RELATION TO SEATING PLANE AND EACH OTHER.
2. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
3. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	22.22	23.24	0.875	0.915
B	6.10	6.60	0.240	0.260
C	3.56	4.57	0.140	0.180
D	0.36	0.56	0.014	0.022
F	1.27	1.78	0.050	0.070
G	2.54 BSC		0.100 BSC	
H	1.02	1.52	0.040	0.060
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	7.62 BSC		0.300 BSC	
M	0°	15°	0°	15°
N	0.51	1.02	0.020	0.040

SOG 20W = -6P
(ML145106-6P)
CASE 751D–04



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029